REMARKS

Claims 5-8 and 10 have been amended and claim 11 has been added in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **June 29, 2006**.

Claims 5-8, 10 and 11 are pending in this application. Claims 1-4 and 9 have been canceled. Claims 5, 6 and 7 have been withdrawn.

Claim Objections

Claim 1 is objected to because of the following informalities: in claim 1, line 8 "via ports" should be –via posts–; and in line 10, "pumps" should be –bumps–. Taking the Examiner's comments into consideration claim 1 has been canceled and new claim 11 added. New claim 11 overcomes the objection to claim 1. Therefore, withdrawal of the objection of claim 1 is respectfully requested.

Claim Rejections under 35 USC §112, Second Paragraph

Claims 1-2 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, the Examiner's objects to the phrase "a via hole into which a via post is filled is arranged in a portion in the insulating film under the connection". Page 9, lines 23-27 of the specification state,

> "Also, via holes 14a to 14d are formed in predetermined portions of the interlayer insulating film 14 on the first wiring patterns 12, and **a via post 11 is filed in the via holes 14a to 14d** respectively."

Therefore, claims 1 and 2 have been canceled and new claim 11 added to indicate that the via post is filed in the via holes.

Further, the Examiner finds confusing the phrase,

> "the electronic parts whose bump is ultrasonic flip-chip packaged to the connection pad;
>
> wherein said via posts in said via holes are positioned at positions corresponding to said bumps of said electronic parts respectively, so that said via ports function as struts which can prevent that said connection pads eat into the insulating film by withstanding pressure or ultrasonic vibration, in case that electronic parts whose pumps are ultrasonic flip-chip packaged to said connection pads"

Taking the Examiner's comments into consideration claims 1and 2 have been canceled and new claim 11 added that overcomes the Examiner's concerns.

Claim Rejections under 35 USC §103(a)

Claims 1-2 and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (U.S. 6,326,561), hereinafter Watanabe in view of Kajiwara et al. (U.S. 6,798,072).

The present invention includes three embodiments. In the first embodiment a wiring substrate (1) is shown having an interlayer insulating film (14) which is formed on the base substrate (10) and a first wiring pattern (12). Via holes (14a to 14d) are formed the interlayer insulating film (14) on the first wiring pattern (12) and via posts (11) is filed in the via holes (14a-14d). Further, a second wiring pattern (12a) is formed on the interlayer insulating film (14) and connected to the via post (11).

As indicated in paragraph 30 of the specification the via holes (14a to 14d) are arranged under the second wiring pattern (12a) which is just under connection pad P. These via holes (14a to 14d) are within a 200 μm of the connection pad P. In this way the via posts (11) in the via holes (14a to 14d) function as struts so that the connection pads P can withstand pressure or ultrasonic vibration applied in the ultrasonic flip-chip packaging process.

Watanabe et al. describes a thin-film multilayer wiring board having a substrate (1) made with an insulating layer (2) formed thereon. In turn a metallic wiring layer (4) is formed on the contacting with the substrate (1) and via holes formed in the insulating layer (2). A number of insulating layers (2) are formed each having a metallic wiring layer (4) laminated thereon. The metallic wiring layers (4) are connected via studs (3) made of a conductive metal filled in the via

holes.

Further, Watanabe et al. states in column 5, lines 42-46 states,

"A number of insulating layers 2 each having a metallic wiring layer thereon are laminated while connecting the metallic wiring layers 4 by via studs 3 made of a conductive metal filled in said via holes and formed by electroless plating."

Kajiwara et al. describes a flip chip assembly structure.

In Watanabe, it is not described that via posts function as struts which can prevent that the connection pads eat into the insulating film by withstanding pressure or ultrasonic vibration, but unexpectedly the via posts 3 are arranged under the bumps 16 of LSI 14.

It seems that the examiner does not admit functional restriction in claims 1 and 2.

Also, as to claims 3 and 4, the Examiner points out that Fig. 5 in Uemematsu et al. (U.S. 6,399,897) shows a semiconductor package with wiring substrate 49, wherein the via hole is a dummy via hole 58a and normal via hole 58 is arranged separately under the wiring pattern connected to the connection pad 60.

But, in Umematsu, when multi-layer wiring pattern is formed by CMP, the dummy signal wiring pattern 54a and the dummy hol 58a connected to it are arranged at peripheral region over the main substrate 12 such that the peripheral region is not polished deeply. The dummy hole 58a is connected to the dummy signal wiring pattern 54a, and is not connected to the normal signal wiring layer 54. This is clear from the purpose of Umematsu and Fig. 5B.

In this application, as shown Fig. 2, the wiring pattern 12a that the via holes (via posts)

functioning as the strut are arranged is normal wiring pattern, and the via holes are arranged in a state that dummy via holes 14d and normal via holes 14a-14c are arranged mixedly. And in the wiring pattern 12a in which the via post 11 in dummy via hole 14d is used as the struts, a normal via hole 14c is arranged separately under the wiring pattern 12 a electrically connected to the dummy via hole 14d.

As mentioned above, in Umematsu, the dummy hole 58a and the dummy signal wiring pattern 54a are only arranged to electrically separate to the normal signal wiring pattern 54 so as to dissolve problem in CMP process.

Accordingly, persons skilled in the art can not anticipate that the via holes are arranged in a state that dummy via holes and normal via holes are arranged mixedly, and a normal via hole is arranged separately under the wiring pattern electrically connected to the dummy via hole, in the wiring pattern in which the via post in dummy via hole is used as the struts.

Therefore, claims 1-4 have been canceled and new claim 11 added to more clearly express the distinctions previously discussed over the prior art. Therefore, withdrawal of the rejection of claims 1-2 and 8 under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (U.S. 6,326,561) in view of Kajiwara et al. (U.S. 6,798,072) is respectfully requested.

Claims 3 and 5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara as applied to claim 1 or 3 above, and further in view of Umematsu et al. (U.S. 6,399,897).

Umematsu et al. describes a multi-layer wiring substrate includes both signal vias (58) and dummy vias (58a).

Claim 3 has been canceled and claim 5 now depends from allowable claim 11. Therefore, withdrawal of the rejection of claims 3 and 5 under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara and further in view of Umematsu et al. (U.S. 6,399,897) is respectfully requested.

Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara as applied to claim 1 above, and further in view of Ohuchi (U.S. 6,590,287).

Ohuchi describes a packaging structure for a semiconductor device uses gold bumps.

Claim 10 is allowable by virtue of its dependence from allowable independent claim 11. Therefore, withdrawal of the rejection of claim 10 under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara and further in view of Ohuchi (U.S. 6,590,287) is respectfully requested.

Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara as applied to claim 1 above, and further in viewof Umematsu and Minagawa et al. (JP-2002009444).

Minagawa et al. describes a ceramic multilayer interconnection board in which dummy vias and normal vias are intermixed.

Claim 4 has been canceled. Therefore, withdrawal of the rejection of claim 4 under 35

U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara and further in viewof Umematsu and Minagawa et al. (JP-2002009444) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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